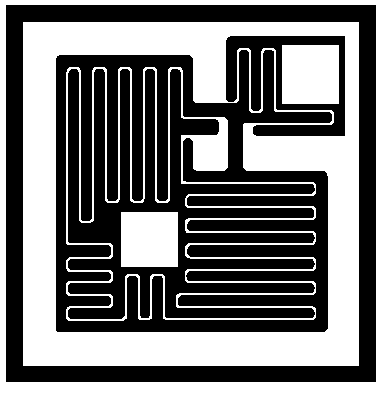
Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.037”**

**.037”**



**B**

**E**

**CHIP BACK IS COLLECTOR**

**Top Material: Al**

**Backside Material: Au**

**Bond Pad Size: .007” X .007”**

**Backside Potential: Collector**

**Process: 06**

**APPROVED BY: DK DIE SIZE .037” X .037” DATE: 6/18/21**

**MFG: FAIRCHILD/NSC THICKNESS .008” P/N: 2N7053**

**DG 10.1.2**

#### Rev B, 7/19/02